Notice of Allowability	Application No.	Applicant(s)	
	10/750,364	KREIFELS, JERRY A.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *9/7/2006*.

2. ☒ The allowed claim(s) is/are *1-3,5-8 and 17-25*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Claims 1-3, 5-8, and 17-25 are pending in the instant application. Applicant's amendments and remarks and amendments have been carefully and fully considered, and are persuasive. Accordingly, this application is in condition for allowance.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jeff Waters on 10/12/2006.

Please amend claims 1, 2, 17, 21, and 23 as follows:

1. An apparatus, comprising:

a memory device including a block of memory operable to store data, said memory device being adapted to at least partially erase said block of memory in a first erase cycle and in a second erase cycle subsequent to the first erase cycle, said memory device stores ~~being further adapted to store~~ a first voltage increment threshold count and a second voltage increment threshold count associated with said block of memory, said memory device being further adapted to count a total number of erase

pulses applied to said block of memory, said memory device being further adapted to apply an erase pulse to said block of memory during the first and the second erase cycles having an erase pulse voltage level based at least in part on the total number of erase pulses applied to said block of memory, the first voltage increment threshold count, and a second voltage increment threshold count.

2. The apparatus of claim 1, wherein the first erase pulse applied during the first erase cycle comprises an initial erase pulse applied to said block of memory ~~during the first erase cycle~~.

17. An apparatus, comprising:

a first block of memory operable to store data and to be at least partially erased in a first erase cycle and in a second erase cycle subsequent to the first erase cycle;

a first memory location uniquely associated with said first block of memory, said first memory location being adapted to store an initial erase pulse voltage level for an erase pulse to be applied to said first block of memory during the second erase cycle, and said first memory location stores ~~being adapted to store~~ a first voltage increment threshold count and a second voltage increment threshold count associated with said first block of memory;

a second block of memory operable to store data and to be at least partially erased in a first erase cycle and in a second erase cycle subsequent to the first erase cycle;

a second memory location uniquely associated with said second block of memory, said second memory location being adapted to store an initial erase pulse voltage level for an erase pulse to be applied to said second block of memory during the second erase cycle, and said second memory location stores ~~being adapted to store~~ a first voltage increment threshold count and a second voltage increment threshold count associated with said second block of memory; and,

a processing unit adapted to evaluate erase performance of said first block of memory during the first erase cycle therefor and to evaluate erase performance of said second block of memory during the first erase cycle therefor, said processing unit being further adapted to establish and store the initial erase pulse voltage level of the erase pulse applied to said first memory, and said processing unit being further adapted to establish and store the initial erase pulse voltage level of the erase pulse applied to said second block of memory based at least in part on the evaluated erase performance of said second block or memory.

21. A method for determining the erase performance of a block of memory of a memory device, comprising:

counting a number of erase pulses applied to the block of memory during a first erase cycle;

comparing the number of erase pulses applied to the block of memory during the first erase cycle to a first threshold number of erase pulses;

changing an erase pulse voltage level of ~~the~~ one or more erase pulses applied to the block of memory during a second erase cycle if the number of erase pulses applied to the block of memory during the first erase cycle is not less than the first threshold number of erase pulses;

comparing the number of erase pulses applied to the block of memory during the second erase cycle to a second threshold number of erase pulses; and,

changing the erase pulse voltage level of ~~the~~ one or more erase pulses applied to the block of memory during a third erase cycle if the number of erase pulses applied to the block of memory during the second erase cycle is not less than the second threshold number of erase pulses.

23. The method of claim 21, wherein the erase pulse voltage level applied during the first erase cycle comprises an initial erase pulse voltage level.

Additionally, claims 1-3, 5-8, and 17-25 will be renumbered as follows:

Original	1-3	5-6	7-8	17-24	25
Final	1-3	4-5	7-8	9-16	6

3. The following is an examiner's statement of reasons for allowance:

4. **Claim 1** recites the limitation "*said memory device stores a first voltage increment threshold count and a second voltage increment threshold count associated*

with said block of memory". This limitation, in combination with the other recited limitations of claim 1, is not taught or suggested by the prior art of record.

5. **Claims 2-3, 5-8, and 25** depend from claim 1 and are considered allowable for at least the same reasons as claim 1.

6. **Claim 17** recites the limitations "*said first memory location stores a first voltage increment threshold count and a second voltage increment threshold count associated with said first block of memory*" and "*said second memory location stores a first voltage increment threshold count and a second voltage increment threshold count associated with said second block of memory*". These limitations, in combination with the other recited limitations of claim 17, are not taught or suggested by the prior art of record.

7. **Claims 18-20** depend from claim 17 and are considered allowable for at least the same reasons as claim 17.

8. **Claim 21** recites the limitations "*changing an erase pulse voltage level of one or more erase pulses applied to the block of memory during a second erase cycle if the number of erase pulses applied to the block of memory during the first erase cycle is not less than the first threshold number of erase pulses*" and "changing the erase pulse voltage level of one or more erase pulses applied to the block of memory during a third erase cycle if the number of erase pulses applied to the block of memory during the second erase cycle is not less than the second threshold number of erase pulses"

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brian R. Peugh
Primary Examiner
10/10/08

Jared I Rutz
Examiner
Art Unit 2187

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JIR